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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/743,113	12/22/2003	Kyung Yun Jung	SUN-DA-114T	8491

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EXAMINER	
MONDT, JOHANNES P	
ART UNIT	**PAPER NUMBER**
3663	

DATE MAILED: 08/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/743,113	KJUNG YUN JUNG	
	Examiner	Art Unit	
	Johannes P. Mondt	3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Amendment filed 5/31/06 forms the basis for this office action. In said Amendment applicant substantially amended all pending claims 1-3. Comments on Remarks submitted with said Amendment are included below under "Response to Arguments".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. ***Claims 1-3*** are rejected under 35 U.S.C. 102(e) as being unpatentable over Lehmann et al (US 2004/0217441 A1) (previously cited) in view of Lee (5,208,177), and , in an alternative rejection, in view of Lee (loc.cit.) and Ghandi et al (6,448,631 B2).

Lehmann et al teach (Figure 11; [0109]-[0117]) a semiconductor device ([0054]) comprising:

a capacitor having a bottom electrode (source/drain regions 143, 146, 143a, 146a) ([0106]), a dielectric layer 124, 124a, 124b (anti-fuse layer is a dielectric: see [0004], [0080]; cf. [0106]) and an upper electrode 125, 125a, 125b ([0080] and [0106]) formed on a semiconductor substrate 101 ([0054]);

a first insulating layer 103 ([0110] and [0054]) formed on the semiconductor substrate 101 ([0110] and [0054]) to cover the capacitor (Figure 11): said first insulating

layer can either be defined as the layer portion of 103 with a lateral extent confined to the area of the device components as recited, i.e., the portion underneath 123 in Figure 10, or, in the alternative rejection, as the entire layer 103;

a first plurality of first contact plugs 141 and 144 ([0110] and [0074]) electrically connected to the bottom electrode (141 connected to 143, 144 to 146, 141a to 143a, and 144a to 146a, respectively) (Fig. 11) and a second plurality of first contact plugs (the portions in first insulating layer 103 of ground lines G electrically connected to upper electrodes 125, 125a,.. ([0121] and hence necessarily are at least in part in said first insulating layer because said upper electrodes 125 are in said first insulation layer) of first contact plugs, wherein the first contact plugs belonging to the first plurality are electrically connected to the bottom electrodes, and wherein the first contact plugs of the second plurality are electrically connected to the upper electrodes);

a first metal wiring 105 ([0054] and [0110]) (Figure 4) formed on the first insulating layer (Figure 11) and connected to the upper electrode through the first contact plugs of the first plurality (namely: through 141 and 144);

a second insulating layer 107 ([0110] and [0054]; Figure 11) formed on the first insulating layer 103;

a second contact plug 127 ([0110] and [0054]) formed on the first insulating layer and connected to the upper electrode 125, 125a,..) through the first contact plugs of the second plurality of first contact plugs, namely the portions of G (loc.cit.);

an anti-fuse 126 ([0110] and [0054]) formed in a certain thickness (an anti-fuse without thickness is impossible because thickness is required in the dielectric phase) in

a second via hole (the via hole filled with 161; Fig. 11) of the second insulating layer and electrically connected to the second contact plug (through 161; Figure 11);

a third contact plug 161 ([0110] and [0054]) filling the second via hole on the anti-fuse; and

a second metal wiring (vertical portions of G abutting the upper main surface of said second insulation layer 107; Figure 11) formed on the second insulating layer and electrically connected to the third contact plug (through 127).

Lehmann et al do not necessarily teach the limitation that "the third contact plug is formed within the anti-fuse wherein the third contact plug does not directly contact the second insulating layer".

However, it would have been obvious to include said limitation in view of Lee, who, in a patent on improvements of the programmability of anti-fuse devices (title, abstract and "Field of the Invention"), hence analogous art, teaches the anti-fuse dielectric material to be a conformal outer lining 41 around the upper conductive portion of the anti-fuse 42 (see col. 3, l. 10-20) so as to have sharp edges where the electric field is locally enhanced, resulting in a lower value of the required voltage for anti-fuse action (col. 3, l. 21-30) (Figures 4A and 4B). *Motivation* to include the teaching by Lee in the invention by Lehmann immediately derives from the advantage of not having to apply potentially damaging voltages for anti-fuse action (col. 1, l. 35-50) in addition to obvious cost savings due to lower power requirements. *Combination* of said teaching with said invention leads to meeting said limitation with 42 and 41 being the third contact plug and the anti-fuse material (161 and 126, respectively).

This concludes the rejection over Lehmann et al and Lee based on the definition of the first insulating layer as the portion of 103 underneath 123.

In the alternative interpretation of the first insulating layer as the entire insulating layer 103 beyond the boundaries of the device with elements as claimed, neither Lehmann et al nor Lee necessarily teach the limitation that first metal wiring 105 is "on the first insulating layer" 103.

However, it would have been obvious to include said further limitation in view of Ghandi et al, who, in a patent on local interconnect architecture for capacitor structures (N.B.: source/drain – gate structure 404/406/408 is inherently a capacitor structure) (title, abstract, "Field of the Invention"), hence analogous art, teach the fabrication of metallization lines through deposition on subsequent insulating layers followed by patterning (col. 3, l. 8-47 and Figures 4A and 4B), thus designing each metallization layer to be on the previously deposited insulating layer (Figures 4A and 4B). The limitation is thus seen to be met by conventional cell architecture for local interconnects pertinent to the problem of arranging for local interconnects for capacitor structures, and has the advantage of removing the need for an etching step in the making of said metallization layers. Said advantage is one of time and cost savings in addition to improved integrity of the underlying insulating layers, providing ample motivation to include the teaching by Ghandi et al in the device by Lehmann et al.

On claim 2: second metal wiring as defined above (vertical portion of G abutting upper main surface of 107 as defined above in the discussion of claim 1) is perpendicular to the first metal wiring 105 (see Figure 11).

On claim 3: The device of claim 1 would necessarily have to be formed in order to function. Claim 3 fails to further limit the device of claim 1 other than simply form each of their components.

Response to Arguments

Applicant's arguments filed 5/31/06 have been fully considered but they are not persuasive. In particular,

(a) In response to applicant's argument that "Lehmann et al do not teach that the first metal wiring is formed on the first insulating layer" (Remarks, page 4) Lehmann in another embodiment (Figure 11) do teach the first metal wiring wherever present laterally (for a lateral view see Figure 10) to be on the interface between the first insulating layer and the second insulating layer: see metal wiring 105 in Figure 11. Furthermore, although a difference would still exist if the first insulating layer is to be defined as a layer extending beyond the elements pertinent to the device as claimed, Ghandi et al teach it is conventional to deposit metallization layers on insulating layers followed by their patterning, which to anyone of ordinary skills in the art has the advantage that the integrity of the underlying insulating layer need not be affecting by an etching step, said etching step being in itself a negative factor for cost and time. Therefore, said argument is not persuasive.

(b) Furthermore, in response to applicant's argument that "Lehmann et al do not teach the third contact plug filling the second via hole and formed within the anti-fuse", the newly added limitation in this regard is obvious in view of Lee, who teach the anti-fuse dielectric to be a conformal lining (41)around the upper conductor portion (42) of

said fuse so as to create sharp edges with consequent enhanced electric field strength and thereby lowering the needed voltage for anti-fuse action with the benefit of lowering the risk of damaging the device by applying voltage over and above what is needed for the normal operation of the device (see whole document, especially Figures 4A and 4B in Lee and col. 3, l. 10-31), said benefits offering motivation to include the teaching by Lee in any anti-fuse device. Therefore, said argument is not persuasive.

(c) The device of the combined invention, counter to applicant's argument against rejection of claim 3, has anti-fuse formed in the second via holes and third contact plugs while first and second metal layers are planar in shape and hence must have been planarized in forming the device. Therefore, said argument is not persuasive.

(d) Applicant's argument that Knall et al "fail to provide any motivation to modify Lehmann et al" is not relevant for the rejection as provided, while in the new art, embodiment of Figure 11, the limitation is met by Lehmann et al. Therefore, argument in traverse of claim 2 is both incorrect and moot.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JPM

August 7, 2006

Patent Examiner:

Johannes Mondt (Art Unit: 3663)